Notice of Allowability	Application No.	Applicant(s)	
	10/800,711	HIRATA ET AL.	
	Examiner	Art Unit	
	son t. dinh	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-17*.

3. ☒ The drawings filed on *16 March 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 3/16/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *East search history*.

Son T. Dinh
Primary Examiner

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

The prior art of record fail to teach or suggest a memory device comprising a plurality of word lines, a plurality of bit lines, a plurality of memory cells provided on a semiconductor substrate, each of the memory cells including a MISFET including a first doped layer, a second doped layer and a gate electrode, wherein first and second memory cells of the plurality of memory cells that are adjacent to each other and arranged in the direction in which the bit lines extend, a first dummy gate electrode connected to a first power supply is provided between a first doped layer of a first MISFET in the first memory cell and a first doped layer of a second MISFET included in the second memory cell, the first doped layer of the first MISFET, the first doped layer of the second MISFET and the first dummy gate electrode together constitute a first dummy MISFET which is held OFF during operation (claim 1); a memory device comprising a plurality of word lines, a plurality of bit lines, and a plurality of first memory cells, the first memory cells being provided on a first substrate and each including a MISFET including a first doped layer, a second doped layer and a gate electrode, a circuit block including a MISFET provided in the substrate and a logic circuit, a power supply for supplying a fixed voltage to at least part of the first substrate, wherein for third and fourth memory cells of the plurality of first memory cells that are adjacent to each other and arranged in the direction in which the bit lines extend, a dummy MISFET which includes a dummy gate electrode connected to a first power supply, third doped layer and a fourth doped layer and is held OFF during operation is provided between a

first doped layer of a first MISFET included in the third memory cell and a first doped layer of a second MISFET included in the fourth memory cell.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son Dinh whose telephone number is 571-272-1868. The examiner can normally be reached on 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-1868.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Dinh
April 16, 2005

Son T. Dinh
Primary Examiner